IDEC Chip Design Contest

A Low Power AI Processor for Embedded System

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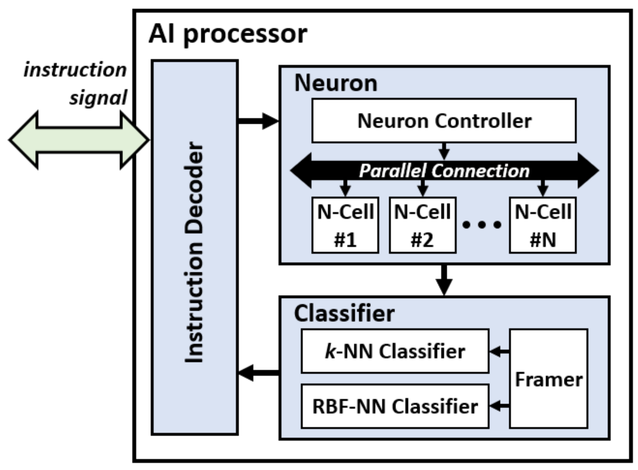
Abstract

We present a low power Artificial Intelligence (AI) processor for embedded system. By designing the neuro-cell (N-Cell) with registers instead of using external memory, the AI processor trains N-Cells rapidly and classifies test data with a less computation and low power consumption. We fabricate the low power and embedded AI processor with Samsung 65 nm RFCMOS technology. The AI processor operates in 1.2V, 50MHz frequency and the circuit is digital type.

AI Processor

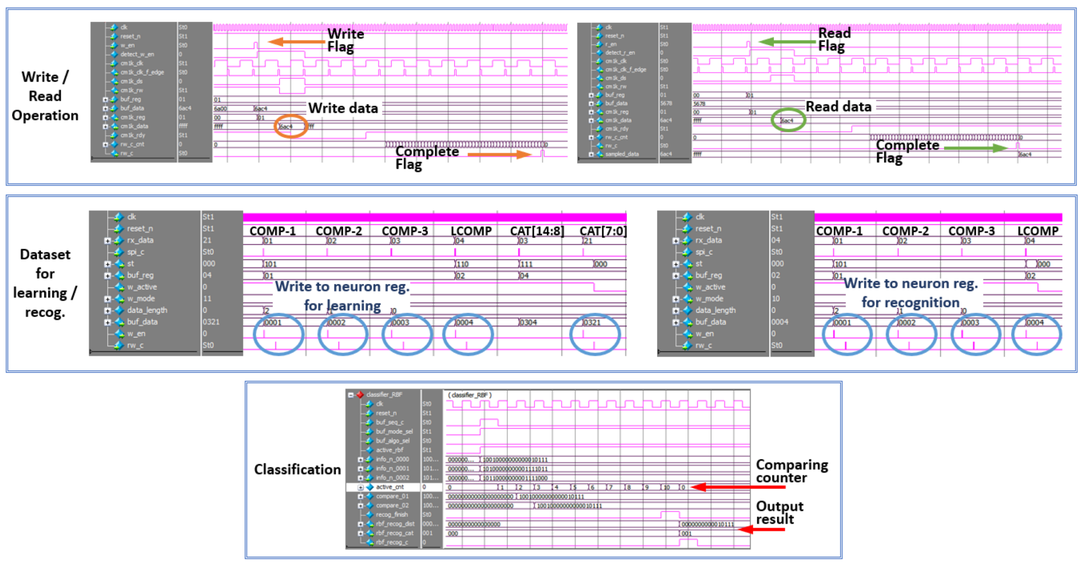
The AI processor receives dataset from the external system and each neuro-cell (N-Cell) stores a training dataset or calculates a distance between the training data and a test dataset in parallel. The calculated distance values are compared each other and the minimum distance is printed out as a result through the serial communication.



[Block diagram of AI processor]

Simulation

Before realizing the AI processor on the FPGA, we simulate our design. The AI processor performs write or read command through the instruction decoder module. With write or read flag, the instruction decoder receives the neuron register and data for writing or reading. After the command, the instruction decoder informs the completer flag for sequential command. To verify the classification result, reading the distance and category value of test data is needed. By confirming the recognition results including the distance and category, we verified the operation of our AI Processor.



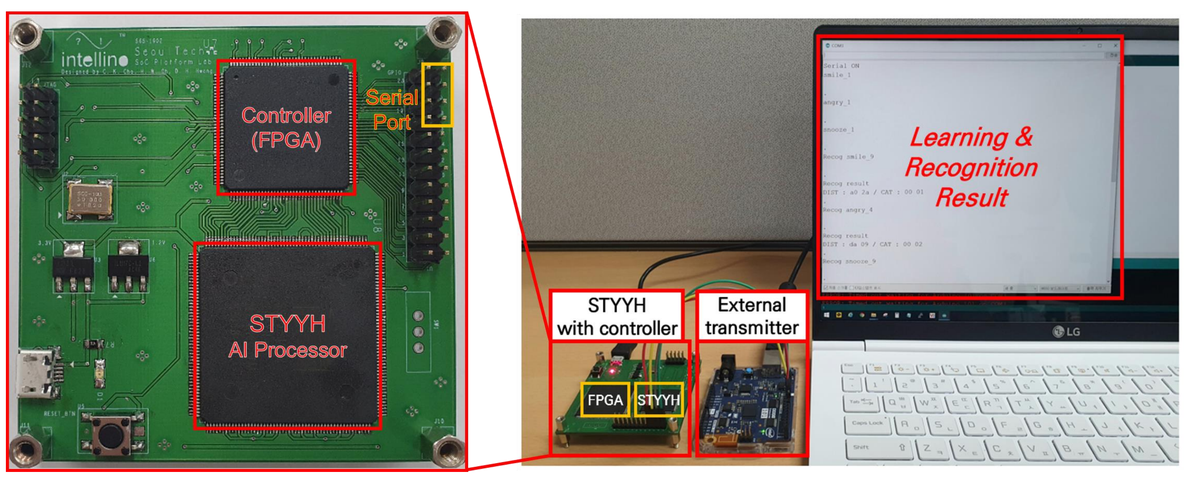
[Development result of AI processor]

FPGA Realization

After the simulation, we realize the design on the FPGA. In order to verify the functionality of the proposed design, featured dataset is set for learning and recognition. We prepare the feature data through the pre-processing that includes cropping, edge detecting, gray-scaling, and featured extracting. As we implemented the designed AI processor and external transmitter only communicates with serial data transmitter, we insert the controller is also implemented on the FPGA with the AI processor. For learning operation, the transmitter generates the test dataset and requests the read command for the recognition results with regard to distance and category. Through the learning and recognition procedure and identifying the result of recognition, we verify the functionality of our design.

Chip Verification

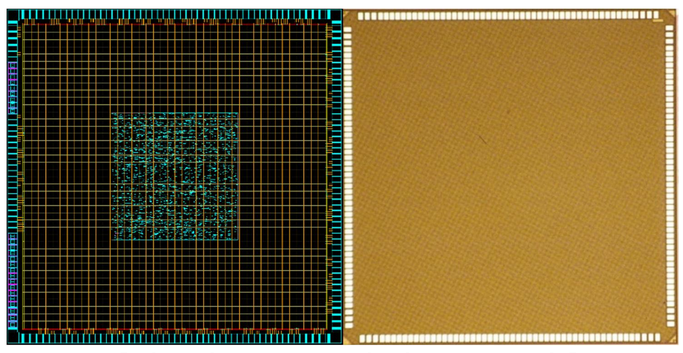
In order to verify the STYYH, we setup an experimental environment that consists of the prototype PCB including STYYH and FPGA for controller, external transmitter. The external transmitter transmits the feature extracted data to the AI processor and receives recognition result through serial port. By checking the result presented with distance and category on the display, we verify the functionality of our chip operation.



[Verification environment with AI processor]

Conclusion

The proposed AI processor was fabricated by using Samsung 65 nm RFCMOS technology. Core size of STYYH is 4mm×4mm and operation frequency is up to 50MHz with 1.2V. For targeting the embedded system, the designed processor operates the learning and recognition locally, with registers, without any memory.



[Chip layout and photograph]

Acknowledgement

This work was supported by IDEC (IC Design Education Center).